17. (amended) A computer, comprising:

means for sampling a temperature level associated with the operation of a central processing unit within said computer;

means for predicting temperature levels associated with the operation of said central processing unit; [within said computer;] and

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

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18. (amended) A computer, comprising:

means for sampling a temperature level associated with the operation of said computer;

means for predicting temperature levels associated with the operation of said computer; and

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

Cancel Claims 60, 64, and 68-70.

REMARKS

Applicant amends Claim 9 better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejection.

Claims 60, 64 and 68 are canceled by this amendment. The double patenting rejection is overcome.

Claims 2-3, 5-6, 9, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 stand rejected under 35 U.S.C. §103 as being unpatentable over Hollowell, II et al. in view of Kikinis and further in view of Gephardt et al.

Independent Claim 5 requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus", and "a clock manager adapted to receive a control signal from said monitor, said clock manager **selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises**

to a level at and above a selected reference temperature level and said CPU is not processing critical I/O".

Independent Claim 6, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed" and "a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager **designating that said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is not processing critical I/O."**

Independent Claim 9, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus" and "a clock manager adapted to receive a control signal from said monitor, said clock manager **reducing central processing unit (CPU) clock speed when said detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O"**.

Applicant agrees with the Examiner's analysis of Hollowell as set forth in the Office Action dated April 28, 1998 (page 3, line 3 – page 4, line 6). Applicant also agrees with the Examiner that Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level (page 4, lines 4-6). Applicant further agrees with the Examiner that Hollowell does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O (page 4, lines 16-18).

While Kikinis teaches that it is known to selectively stop clock signals when the detected temperature rises above a reference temperature level, Kikinis fails to teach or suggest that the selective stopping is performed only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O. Moreover, Kikinis has fails to teach or

suggest any modification of the clock signal to the processor for any reasons other than temperature. Indeed, the Kikinis and Hollowell references, alone or in combination, fail to teach or suggest that critical I/O will, or should, affect the performance of the temperature reduction mechanism.

Gephardt is the reference newly combined with Hollowell and Kikinis. Assuming, arguendo, that Gephardt teaches a power management that monitors CPU activity and dependent upon one of the classifications of activity being detected on table II (col. 9, lines 14-25), can control the frequency of the CPU clock signal and system clock signal as suggested by the Examiner. Not only does Gephardt fail to teach or suggest any means for detecting critical activity - Gephardt fails to mention "critical activity" at all in any context.

Moreover, Gephardt teaches that clock speed is decreased in response to reduced levels of activity – thus lower clock speed for lower level of activity – and higher levels of speed for higher levels of activity. In contrast, the present invention stops (or reduces) clock speed "when said clock speed **rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O**". It would not have been obvious to one having ordinary skill in the art at the time the invention was made to combine Gephardt with Kikinis and Hollowell and modify the resulting device so that the resulting temperature reduction mechanism will selectively stop (or reduce) the clock signal to the CPU only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O.

The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Applicants' claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellants' disclosure to obviate their claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect

Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. §103 rejection is overcome. Just because something is desirable (especially in hindsight) does not mean it is obvious.

Claims 2, 3, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the apparatus of Claim 5 wherein said user input is coupled to a keyboard. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 3 further defines the apparatus of Claim 5 wherein said output is coupled to a display device. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 34 further defines the apparatus of Claim 5, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 35 further defines the apparatus of Claim 9, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

Claim 36 further defines the apparatus of Claim 6, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in

combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 37 further defines the apparatus of Claim 6, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 38 further defines the apparatus of Claim 5, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 39 further defines the apparatus of Claims 9, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

Claim 41 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 42 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 43 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt

references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 45 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 46 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 47 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 49 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 50 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 51 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The

Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 53 further defines the apparatus of Claim 37, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 54 further defines the apparatus of Claim 38, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 55 further defines the apparatus of Claim 39, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 57 further defines the apparatus of Claim 6, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 58 further defines the apparatus of Claim 5, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 59 further defines the apparatus of Claim 9, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 61 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 57.

Claim 62 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 58.

Claim 63 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 59.

Claim 65 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 57.

Claim 66 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 58.

Claim 67 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 59.

Claim 71 further defines the apparatus of Claim 11, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 11.

Claim 72 further defines the apparatus of Claim 5, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 73 further defines the apparatus of Claim 9, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

Claims 17-21, 23, and 69-70 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hollowell, et al in view of Kikinis and further in view of Chen et al.

Independent 17, as amended, requires and positively recites, "means for **sampling a temperature level** associated with the operation of a central processing unit within said computer", "means for **predicting temperature levels associated with the operation of said central processing unit within said computer**" and "means **for using said prediction for automatic control of temperature within said computer**, said temperature control remaining transparent to a user of said computer".

Independent Claim 18, as amended, requires and positively recites, "means for **sampling a temperature level** associated with the operation of said computer", "means **for predicting temperature levels associated with the operation of said computer**" and "means for **using said prediction for automatic temperature control within said computer**, said temperature control remaining transparent to a user of said computer".

Independent Claim 21, as amended, requires and positively recites, "a central processing unit (CPU)", "means for **sampling a temperature level** within said apparatus" and "means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) **to maintain said temperature level**

within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O".

Applicant agrees with the Examiner that Hollowell and Kikinis "do not teach predicting temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control" (Office Action dated April 28, 1998 (page 8, lines 4–6). Applicant also agrees with the Examiner that Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level (page 4, lines 4-6) and does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O (page 4, lines 16-18).

The Chen reference teaches a temperature control system which employs feedback to adjust the output count signal (col. 2, lines 43-44) in which NO TEMPERATURE MEASUREMENTS ARE NEEDED OR MADE (col. 2, lines 44-45).

Thus, it would not be obvious to one of ordinary skill in the art without improper hindsight to combine the teachings of Chen with Hollowell and Kikinis, and thereafter modify the resulting apparatus to be an apparatus that both samples the temperature within the computer (or cpu) and there after uses the temperature sample in predicting temperature levels associated with the operation of a computer (or cpu).

As a result, any combination of the Hollowell, Kikinis and Chen references fails to teach or suggest, "means for **sampling a temperature level** associated with the operation of a central processing unit within said computer", "means for **predicting temperature levels associated with the operation of said central processing unit within said computer**" and "means **for using said prediction for automatic control of temperature within said computer**", as required by Claim 17, or "means for **sampling a temperature level** associated with the operation of said computer", "means **for predicting temperature levels associated with the operation of said computer**" and "means for **using said prediction for automatic temperature control within said computer**", as required by Claim 18.

Independent Claim 21 requires and positively recites, "a central processing unit (CPU)", "means for **sampling a temperature level** within said apparatus" and "means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) **to maintain said temperature level within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O**".

As stated above, Chen teaches a temperature prediction mode in which in which NO TEMPERATURE MEASUREMENTS ARE NEEDED OR MADE (col. 2, lines 44-45).. Kikinis, on the other hand, discloses a device in which temperature measurements ARE MADE – i.e., which selectively stops clock signals when the detected temperature rises above a reference temperature level. Kikinis fails, however, to teach or suggest that the selective stopping be performed only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O. Kikinis also fails to teach or suggest any modification of the clock signal to the processor for any reasons other than temperature. Any combination of Chen, Kikinis and Hollowell, fails to address the discrepancies between, or justify any combination of the Chen and Kikinis (regarding temperature measurements and temperature prediction) with the Hollowell reference. Moreover, none of the references (alone or in combination) teach or suggest that critical I/O will, or should, affect the performance of the temperature reduction mechanism.

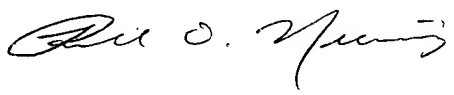
As stated previously, the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Applicants' claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellants' disclosure to obviate their claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose

among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. §103 rejection is overcome.

Claim 23 stands allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claims 2, 3, 5, 6, 9, 11, 16-19, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand allowable and the application is in allowable form. Applicants respectfully request withdrawal of the rejections and allowance of the application.

Respectfully submitted,



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